DECISION DIRECTED PHASE LOCKED LOOPS (DD-PLL) WITH EXCESS PROCESSING POWER IN DIGITAL COMMUNICATION SYSTEMS

ABSTRACT OF THE DISCLOSURE

A decoder of a data signal subjected to phase shifting keying (PSK) modulation uses a plurality of phase locked loops (801-1to 801-n) having an inner decoder for short block codes, at least one of which is adapted to apply excess processing power to process a selected burst of the data signal, such as processing the burst with multiple initial phase/frequency error estimates. A selection circuit identifies the burst and supplies to said one of said plurality of phase-locked loops (801-1 to 801-n) for re-processing the burst with excess processing power. An outer Reed-Solomon block decoder (319) may be used to correct errors in the codewords from the phase locked loops and may be used in the selection of the burst by the selection circuit.